

11. (Amended) A fabrication method of a semiconductor device comprising the steps of:

- (a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips;
- (b) applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate;
- (c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by [beating] heating means and aligning the semiconductor chips to the mounting parts of the substrate at a first stage by a bonding head [to which the semiconductor chips are absorbed] which also holds the semiconductor chips on the substrate with pressure;
- (d) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive; and
- (e) thereafter heating the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, where the heating is performed with a pressure applied to the semiconductor chips.

12. (Amended) A fabrication method according to claim 11, wherein in the heating step

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- (c), heating the thermosetting insulating adhesive is performed by a heat plate on which the substrate [mounting the semiconductor chips] is placed.

15. (Amended) A fabrication method of a semiconductor device comprising the steps of:

(a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips;

(b) applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate;

(c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by heating means and, then, aligning the semiconductor chips to the mounting parts of the substrate at a first stage and performing a first fixing of the semiconductor chips with a first pressure by a bonding head to which the semiconductor chips are absorbed;

(d) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive; and

(e) thereafter heating, at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips with a second pressure, wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips.

16. (Amended) A fabricating method according to claim 15, wherein in the heating step

(c), heating the thermosetting insulating adhesive is performed by a heat plate on which the substrate [mounting the semiconductor chips] is placed.

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17. (Twice Amended) A fabrication method according to claim 15, wherein in the heating step (e), heating the thermosetting insulating adhesive is performed by a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate.

REMARKS

Claims 3-6 and 8-17 are pending in this application, of which claims 9-10 have been withdrawn from consideration, leaving only elected claims 3-6, 8 and 11-17 under consideration.

Claims 11-12 and 15-17 have been amended. No new claims have been added.

Fig. 3 has been corrected to correct a misspelling, as pointed out by the Examiner. If approved, this correction will be incorporated into formal drawings to be filed prior to payment of the Issue Fee.

Claims 3, 4, 12 and 16 stand rejected under 35 U.S.C. §112, second paragraph as indefinite.

Accordingly, claims 11-12 and 15-17 have been amended to correct the noted instances of indefiniteness. Claim 15, from which claims 3-4 depend, have been amended to provide proper antecedent basis for the recited terms "said second fixing" and "said second pressure".

Thus, the §112, second paragraph, rejection should be withdrawn.

The Examiner has rejected the claims as follows:

1. Claims 11, 13 and 15 under 35 USC §102(b) as anticipated by JP 58180091 to Maeda (hereinafter "Maeda");
2. Claims 5, 6, 8, 11 and 15 under 35 USC §103(a) as unpatentable over Applicants' Admitted Prior Art (hereinafter "APA") in view of Maeda;